WHAT IS CLAIMED IS:

1. A semiconductor chip comprising:

(a) a semiconductor substrate of a first conductivity type having an active surface having therein an interior active region containing integrated circuitry;

(b) a peripheral barrier region of a second conductivity type disposed in the semiconductor substrate adjacent to the active region;

(c) a voltage conductor for applying a non-foreword biasing voltage to the barrier region;

(d) a plurality of solder bumps disposed on the active surface and electrically coupled to various conductors of integrated circuitry in the active region, respectively, the solder bumps being adapted for attachment to a plurality of conductive pads, respectively, of a mounting substrate;

(e) wherein a substantial amount of photon-induced current caused by ambient light impinging on the exposed edges and/or surfaces of the semiconductor substrate is collected by the barrier region and substantially less of the photon-induced current is collected by any of the integrated circuitry.

2. The semiconductor chip of claim 1 wherein the barrier region surrounds the interior active region.

3. The semiconductor chip of claim 1 wherein the voltage conductor applies a reverse bias voltage to the barrier region.

4. The semiconductor chip of claim 1 wherein the voltage conductor applies a zero bias voltage to the barrier region.

5. The semiconductor chip of claim 1 including a layer of light barrier material on a back surface of the semiconductor substrate.

6. A semiconductor chip comprising:

(a) a P-type semiconductor substrate having an active surface having therein an interior active region containing integrated circuitry and a back surface having a light barrier coating thereon;

(b) a peripheral N-type barrier region disposed in the semiconductor substrate surrounding the active region;

(c) a supply voltage conductor for applying a reverse bias voltage to the N-type barrier region;

(d) a plurality of solder bumps disposed on the active surface and electrically coupled to various conductors of integrated circuitry in the active region, respectively, the solder bumps being adapted for attachment to a plurality of conductive pads, respectively, of a mounting substrate;

(e) wherein a substantial amount of photon-induced current caused by ambient light impinging on the exposed edges and/or surfaces of the semiconductor substrate is collected by the N-type barrier region and substantially less of the photon-induced current is collected by any of the integrated circuitry.

7. The semiconductor chip of claim 2 wherein the barrier region surrounds the interior active region.

8. The semiconductor chip of claim 2 wherein the integrated circuitry includes an amplifier having a first input connected to both the cathode of the first input protection diode and a first solder bump and a second input connected to both the cathode of the second input protection diode and a second solder bump, wherein an total input bias current of the amplifier includes relatively little photon-induced current.

9. The semiconductor chip of claim 2 wherein the supply voltage conductor is coupled to the N-type barrier region by means of an N+ contact region on the N-type barrier region.

10. The semiconductor chip of claim 2 wherein at least one of the solder bumps overlies the barrier region.

11. A semiconductor chip comprising:

(a) a P-type semiconductor substrate having an active surface having therein an interior active region containing integrated circuitry and a back surface having a light barrier coating thereon;

(b) a peripheral N-type barrier region disposed in the semiconductor substrate surrounding the active region;

(c) a supply voltage conductor for applying a reverse bias voltage to the N-type barrier region;

(d) a plurality of solder bumps disposed on the active surface and electrically coupled to various conductors of integrated circuitry in the active region, respectively, the solder bumps being adapted for attachment to conductive pads, respectively;

(e) a mounting substrate having thereon a plurality of conductive pads to which the solder bumps are physically and electrically connected, respectively;

(f) wherein a substantial amount of photon-induced current caused by ambient light impinging on the exposed edges and/or surfaces of the semiconductor substrate is collected by the N-type barrier region and substantially less of the photon-induced current is collected by

any of the integrated circuitry.

12. A method of reducing the amount of photon-induced current in a semiconductor chip, comprising:

(a) forming a peripheral N-type region in a P-type substrate of the chip, the N-type region adjacent to an active region including integrated circuitry on a first surface of the substrate and reverse biasing a PN junction between the N-type region and the P-type substrate;

(b) providing a plurality of solder bumps on the active surface and electrically coupling of solder bumps to various conductors, respectively, of the integrated circuitry in the active region, the solder bumps being adapted for attachment to conductive pads of a mounting substrate, respectively; and

(c) collecting nearly all photon-induced current caused by ambient light impinging on the exposed edges of the semiconductor substrate by means of the N-type barrier region so that relatively little of the photon-induced current is available to be collected by any of the integrated circuitry.

13. The method of claim 12 wherein step (a) includes forming the peripheral N-type region in a P-type substrate of the chip, the N-type region to surround the active region.

14. The method of claim 12 including mounting the chip on a mounting substrate by physically and electrically attaching the solder bumps to corresponding conductive metal pads on a surface of the mounting substrate.

15. A method of reducing the amount of photon-induced current in a semiconductor chip, comprising:

(a) forming a peripheral N-type region in a P-type substrate of the chip, the N-type region surrounding an active region including integrated circuitry on a first surface of the substrate and reverse biasing a PN junction between the N-type region and the P-type substrate;

(b) providing a plurality of solder bumps on the active surface and electrically coupling of solder bumps to various conductors, respectively, of the integrated circuitry in the active region;

(c) mounting the chip on a mounting substrate by physically and electrically attaching the solder bumps to corresponding conductive metal pads on a surface of the mounting substrate.

(d) collecting nearly all photon-induced current caused by ambient light impinging on the exposed edges of the semiconductor substrate by means of the N-type barrier region so that relatively little of the photon-induced current is available to be collected by any of the integrated circuitry.

16. A semiconductor device structure for reducing the amount of photon-induced current in a semiconductor chip, comprising:

(a) peripheral barrier region means in a P-type substrate of the chip, adjacent to an active region including integrated circuitry on a first surface of the substrate, for collecting nearly all photon-induced current caused by ambient light impinging on an exposed edge of the semiconductor substrate so that relatively little of the photon-induced current is available to be collected by the integrated circuitry;

(b) means for biasing a PN junction formed by the N-type region and the P-type substrate to a reverse bias or zero bias value; and

(c) a plurality of solder bumps on the active surface and electrically coupled to various conductors, respectively, of the integrated circuitry in the active region, the solder bumps being adapted for attachment to conductive pads, respectively.

17. The semiconductor device structure of claim 16 including a mounting substrate and the solder bumps electrically physically connected to corresponding conductive metal pads on a surface of the mounting substrate.